

Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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AD1847/ADSP-2181 Daisy Chain Tips & Tricks

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Overview

This Engineer's Note will focus on questions that may arise when interfacing multiple AD1847s to an ADSP-21xx device while operating in '1-wire' mode. Specifically, tips for proper sequence for changing the crystal input 'on the fly' will be presented.

Problem Description

I am interfacing a 2181 with two AD1847 SoundPort Codecs. The 1847s are daisy chained with one master and one slave. The 1847s are operated in 1 wire mode and is interfaced to SPORT0 (of the 2181) is in multi-channel mode. The serial communication always will stay in 1 wire mode. The code I am developing initializes the slave first (via the appropriate time slots) while leaving the master in the default state after reset. It then initializes the master.

After everything is done an analog loopback test is conducted on the slave to verify proper functionality. However, the analog loopback test is failing approximately 1 in 8 times. Our analog loopback test consists to writing a near full scale positive value out and verifying that a large value returns. The large value comparison reference is no where near full scale to allow for subtle gain differences. Part of the initialization involves changing the XTAL reference and sample rate to 44.1. The data sheet states that such changes should occur simultaneously with the master but if not possible the slave should be changed first. This makes me a little suspicious of changing the slave first. Can you shed some light on the following:

Can the slave xtal and sample rate change before the master?

What is the effect of changing the slave sample rate to 44.1 XTAL2 when the master is still providing a XTAL1 clock to the slave?

Changing slave sample rate and crystal selection before master could be the cause of your random failures. Is it possible to change the both at the same time? The change doesn't really take place until the MCE bit in the control register is released. Is it possible to change the sample

rate and crystal selects on different frames with MCE asserted and then release both MCE's on the same frame?

You could try changing the master codec clock and sample rate register before the slave's. This could cause you to get bogus data for the first few frames, but may run more predictably.

Why does the master provide a 12.288 MHz clock on the clockout pin when it is in XTAL1 mode? Does this prevent the slave from operating at 48KHz? Remember, the master uses the 2x12.288 XTAL1 frequency at 48 KHz.

The slave can be run at 48 kHz. The short answer is, the master codec divides the XTAL1 input by 2 before using it (12.288mhz). Slave codecs use the XTAL2 input only and do not do a divide by two before using it and only need the 12.288 MHz clock. Table below tries to explain this.

MASTER CODEC:

mode	input pin	input clock	clock gen ops	internal compute	clock
XTAL1	XTAL1	24.576	/2	*2	24.576 MHz
XTAL2	XTAL2	16.9344	/1	*1.5	25.4016 MHz

SLAVE CODEC:

mode	input pin	input clock	clock gen ops	internal compute	clock
XTAL1	XTAL2	12.288	/1	*2	24.576 MHz
XTAL2	XTAL2	16.9344	/1	*1.5	25.4016 MHz

After the XTAL is changed there is a small time window before the INIT pin goes high. Can this window be used to send an additional config command to the 1847?

We would not recommend that. If you are changing the configuration, you should put the part into MCE. Change everything that needs to be changed. Change the sample rate and crystal selects and then release MCE.